Claims

1. An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a layer composed of the compounds of gallium and oxygen including but not limited to mixtures of Ga_2O_3, Ga_2O and other gallium oxygen compounds positioned on upper surface of said compound semiconductor wafer structure;

a second insulating layer composed of the compounds of gallium and oxygen and at least one or more rare earth elements that form an insulating layer deposited on top of the initial supporting gallium oxygen layer, with said first and second layers forming a gate insulator structure adjacent to and on top of the compound semiconductor structure;

a stable refractory metal gate electrode positioned on upper surface of said gate insulator structure layers;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;

wherein the refractory metal gate electrode comprises a refractory metal selected from the group consisting of W, WN or WSi or combinations thereof;

means of interconnection of said transistors forming a monolithically integrated circuit.

2. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the initial layer of gallium oxygen compounds forms an atomically abrupt interface with the upper surface of the compound semiconductor wafer structure.

3. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the gate insulator structure is composed of three layers, an initial gallium oxygen compound layer, a graded layer that contains varying compositions of gallium oxygen and at least one rare-earth element, and a third insulator layer that is composes largely of a compound of gallium, oxygen and one or more rare earth elements.

4. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the gate insulator structure is composed of more than three multiple layers, an initial gallium oxygen compound layer, and multiple layers containing gallium and oxygen with or without the inclusion of one or more rare earth elements that together form an insulating gallium oxide gate insulator structure.

5. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the initial gallium oxygen compound layer has a thickness of more than 10 angstroms and less than 25 angstroms.

6. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the gate insulator structure has an overall total thickness of 20-300 angstroms.

7. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the initial gallium oxygen compound layer forms an atomically abrupt interface with the compound semiconductor structure that extend less than four atomic layers in depth of structural interface modulation.

8. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the initial gallium and oxygen compound layer and the gate insulator structure protects the upper surface of the compound semiconductor wafer structure.

9. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the refractory metal gate electrode comprises a refractory metal which is stable in presence of the top layer of the gate insulator structure at an elevated temperature of 700°C and above.

10. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the source and drain ion implants comprising said enhancement mode metal-oxide-compound semiconductor field effect transistor being an n-channel device or p-channel device.

11. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the source and drain ion implants comprise and Be/F or C/F, said enhancement mode metal-oxide-compound semiconductor field effect transistor being a p-channel device.

12. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the upper surface of the compound semiconductor wafer structure comprises GaAs.

13. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1 wherein the upper surface of the compound semiconductor wafer structure comprises $In_xGa_{1-x}As$.

14. An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a layer composed of the compounds of gallium and oxygen compounds including but not limited to mixtures of Ga_2O_3, Ga_2O and other gallium oxygen compounds positioned on upper surface of said compound semiconductor wafer structure;

a second insulating layer deposited upon the first composed of the compounds of gallium and oxygen and at least one or more rare earth elements such that the normalized relative composition of gallium, oxygen, and one or more rare earth elements are changing in a monotonic manner as a function of the thickness within said insulating layer;

a third insulating layer deposited on top of said second layer composed of gallium oxygen and at least one or more rare earth elements wherein said first, second and third layers form a gate insulator structure adjacent to and deposited on top of the compound semiconductor structure;

a stable refractory metal gate electrode positioned on upper surface of said gate insulator structure layers;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas;

wherein the refractory metal gate electrode comprises a refractory metal selected from the group consisting of W, WN or WSi or combinations thereof;

means of interconnection of said transistors forming a monolithic integrated circuit.

15. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14 wherein the initial layer of gallium oxygen compounds forms an atomically abrupt interface with the upper surface of the compound semiconductor wafer structure.

16. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14 wherein the gate insulator structure is composed of three or more layers, an initial gallium oxygen compound layer, a graded layer that contains varying compositions of gallium oxygen and at least one rare-earth element, and a third insulator layer that is composes largely of a compound of gallium, oxygen and one or more rare earth elements.

17. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14 wherein the initial gallium oxygen compound layer has a thickness of more than 10 angstroms and less than 25 angstroms.

18. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14 wherein the gate insulator structure has an overall total thickness of 20-300 angstroms.

19. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14 wherein the initial gallium oxygen compound layer forms an atomically abrupt interface with the compound semiconductor structure that extend less than four atomic layers in depth of modulation of said interface.

20. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14 wherein the initial gallium and oxygen compound layer and the gate insulator structure protects the upper surface of the compound semiconductor wafer structure.

21. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14 wherein the refractory metal gate electrode comprises a refractory metal which is stable in presence of the top layer of the gate insulator structure at an elevated temperature of 700°C and above.

22. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14 wherein the source and drain ion implants comprising said enhancement mode metal-oxide-compound semiconductor field effect transistor being an n-channel device.

23. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14 wherein the source and drain ion implants comprise and Be/F and C/F, said enhancement mode metal-oxide-compound semiconductor field effect transistor being a p-channel device.

24. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14 wherein the upper surface of the compound semiconductor wafer structure comprises GaAs.

25. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 14 wherein the upper surface of the compound semiconductor wafer structure comprises $In_xGa_{1-x}As$.

26. An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a multilayer gate insulator structure composed of alternating layers comprised of gallium, oxygen, at least one rare-earth element forming a gate insulator with low electronic midgap defect density positioned on upper surface of said compound semiconductor wafer structure;

a stable refractory metal gate electrode positioned on upper surface of said gate insulator structure layer;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas,

wherein dielectric spacers are positioned on sidewalls of the stable refractory gate metal electrode.

27. An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure positioned on upper surface of said compound semiconductor wafer structure;

a stable refractory metal gate electrode positioned on upper surface of said gate insulator structure;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas,

wherein the compound semiconductor wafer structure comprises a wider band gap spacer layer and a narrower band gap channel layer.

28. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 27 wherein the wider band gap spacer layer is positioned between the gate oxide layer and the narrower band gap channel layer.

29. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 27 wherein the wider band gap spacer layer has a thickness of between 3-200 angstroms

30. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 27 wherein the wider band gap spacer layer comprises either $Al_xGa_{1-x}As$, InP, or $In_zGa_{1-z}P$ or a combination thereof.

31. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 27 wherein the narrower band gap channel layer has a thickness of 10-300 angstroms.

32. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 27 wherein the narrower band gap channel layer is positioned between the wider band gap spacer layer and a buffer layer.

33. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 27 wherein the narrower band gap channel layer comprises $In_yGa_{1-y}As$.

34. An enhancement mode metal-oxide-compound semiconductor field effect transistor comprising:

a compound semiconductor wafer structure having an upper surface;

a gate insulator structure positioned on upper surface of said compound semiconductor wafer structure;

a stable refractory metal gate electrode positioned on upper surface of said gate insulator structure layer;

source and drain ion implants self-aligned to the gate electrode; and

source and drain ohmic contacts positioned on ion implanted source and drain areas,

wherein the compound semiconductor wafer structure comprises a Al_xGa_{1-x} As, $In_yGa_{1-y}As$, InP, or $In_zGa_{1-z}P$ layer, said layer being positioned on upper surface of a compound semiconductor substrate.

35. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 34 wherein the compound semiconductor substrate includes a GaAs based semiconductor wafer.

36. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 34 wherein the compound semiconductor substrate includes a InP based semiconductor wafer.

37. An enhancement mode metal-oxide-compound semiconductor field effect transistor as claimed in claim 1, 13, 26, and 33 that may be integrated together with similar and complementary transistor devices to form complementary metal-oxide compound semiconductor integrated circuits.

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